IN THE CLAIMS

Kindly replace the claims of record with the following full set f claims:

1. (Currently amended) A data processing system compri ng:

memory device and a plurality of data processors ~~provi~~ ~~ed for~~ accessing [[to]] said memory device,

at least one local memory unit associated with correspo ding ones of said plurality of data processors, said local memory unit adapted to e selectively accessed by a memory access request of said corresponding data processor wherein said memory device and said local memory unit have a single address space nd an address range within said single address space distinguishes between a meme y access to said memory device and said local memory unit, ~~wherein~~

a communication interface [[is]] coupled between said emory device and said plurality of data processors and said at least on e local memory nit, said communication interface including:

a network of nodes and a memory interface, each node comprising at least one slave port for receiving a memory access request from a data p ocessor or from a previous node and at least one master port for issuing a memo access request to a next node or to said memory device in accordance with the memor access request received at said slave port, wherein one or more slave ports are connected o a master port of a previous node, wherein one or more slave ports are connected o one of said data processors, wherein one or more master ports are connected to a slave port of a next node, wherein one or more master ports are connected to [[the a memory interface, wherein the memory interface arbitrates access to the memory levice and said at least one local memory unit, wherein the communication interface positioned on a single chip, and wherein the memory device is not positioned on the ingle chip~~, wherein said communication interface further includes at least one local m nory unit adapted to be selectively accessed by a memory access request, wherein sai memory device and said local memory unit have a single address space and an address ange within said single address space distinguishes between said memory device and aid local memory~~.

2. (Previously presented) The data processing system acc ding to claim 1, wherein at each node the number of said slave ports is higher than the n nber of said master ports.

3. (Previously presented) The data processing system acc ding to claim 1, wherein said network of nodes is hierarchically structured.

4. (Previously presented) The data processing system ac rding to claim 3, wherein said network of nodes is arranged in a directed acyclic graph st icture.

5. (Previously presented) The data processing system acc rding to claim 4, wherein said network of nodes is arranged in a tree structure.

6. (Previously presented) The data processing system ac rding to claim 1, wherein said network of nodes include n groups of nodes with $n \geq 2$, w erein each of the slave ports of the nodes of a first group is connected to one of said p rality of data processors, the master ports of the nodes of the n^{th} group are coupled to sa l memory device, and each of the slave ports of the nodes of the n^{th} group is connect l to a master port of the nodes of the $(n-1)^{th}$ group.

7. (Previously presented) The data processing system ac rding to claim 1, wherein said nodes are hubs.

8. (Cancelled).

9. (Previously presented) The data processing system ac rding to claim 1, wherein at least one node further comprises at least one memory port t which a local memory unit is connected.

10. (Previously presented) The data processing system ac rding to claim 1, wherein said communication interface includes a cache controller for ntrolling at least a section

of the local memory unit as a cache memory.

11. (Previously presented) The data processing system acc· ding to claim 1, wherein said communication interface further includes at least one sync ·onization means for streaming communication between data processors.

12. (Previously presented) The data processing system acc ·ding to claim 11, wherein at least one node includes said synchronization means ɔr streaming communication between the data processors directly or indirec y coupled to said nodes.

13. (Previously presented) The data processing system acc rding to claim 11, wherein the local memory unit is configured to provide storag ɔased on a first-in/first-out function and said synchronization means comprises a first- ı/first-out administration means for controlling said local memory unit.

14. (Cancelled).

15. (Previously presented) The data processing system ac· ırding to claim 1, wherein at least a portion of said plurality of data processors is positioı d on said single chip.